

```

graph TD
    Host[Host 4] --- HPC[Host Protocol Chip 30]
    subgraph Storage_Controller [Storage Controller 8]
        HPC --- Processor[Processor 10]
        HPC --- IOM[I/O Manager 14]
        subgraph IOM_Box [I/O Manager 14]
            HB[Host Bus 20]
            DMA[DMA Controller 26]
            IML[I/O Manager Control Logic 28]
            MI[Memory Interface 24]
            SB[Storage Bus 22]
        end
        Processor --- Cache[Cache 12]
        MI --- Cache
    end
    IOM_Box --- SB
    SB --- SPC[Storage Protocol Chip 32]
    SPC --- SD[(Storage Device 6)]

```

30

THE UNIVERSITY OF CHICAGO

FIG.3

60

ADDRESS FORMAT	
Bit Offset	Field Description
63	Reserved
62	Hardware Control Block enabled (0 - do not use HCB; 1 - use HCB index
61-64	Hardware Control Block Index.
43-33	Reserved
32-0	Memory Address

001000" 8220E960

FIG.4

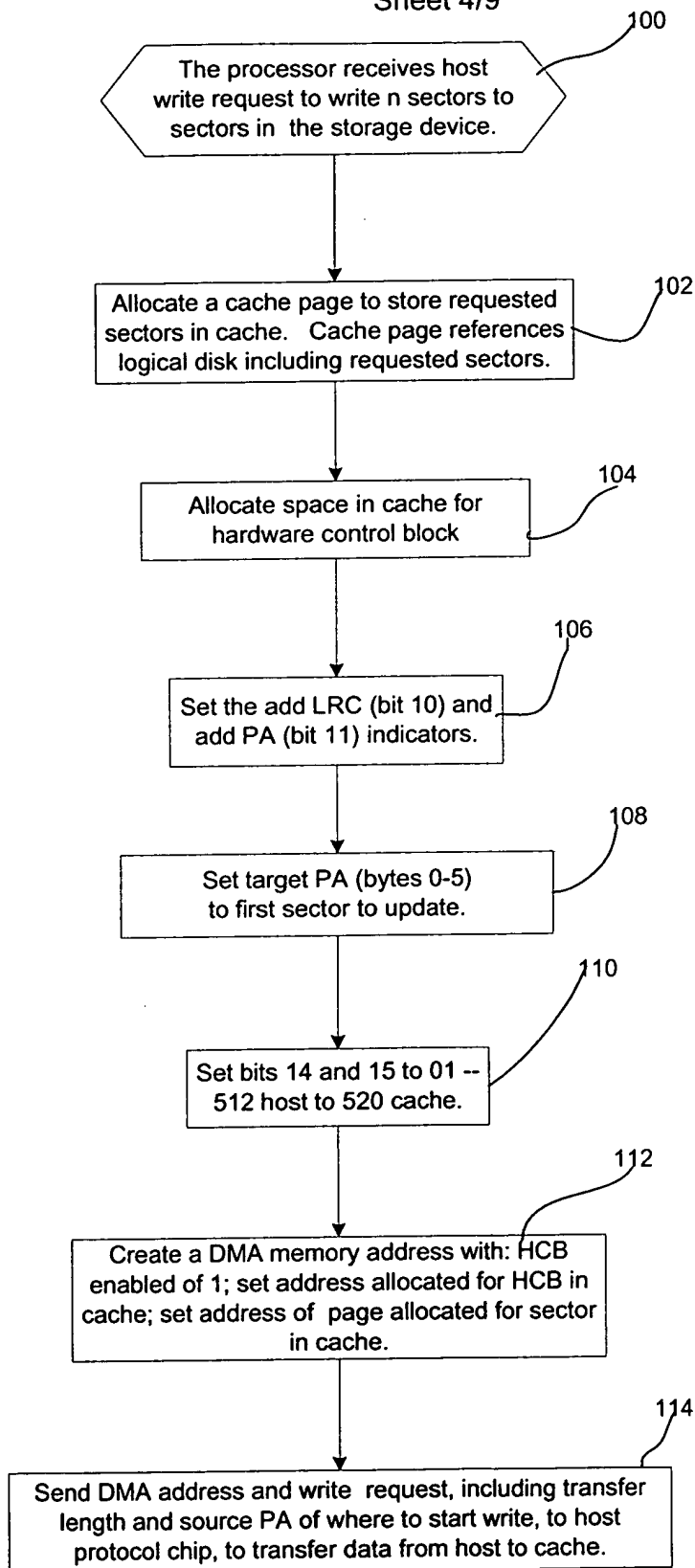


FIG.5

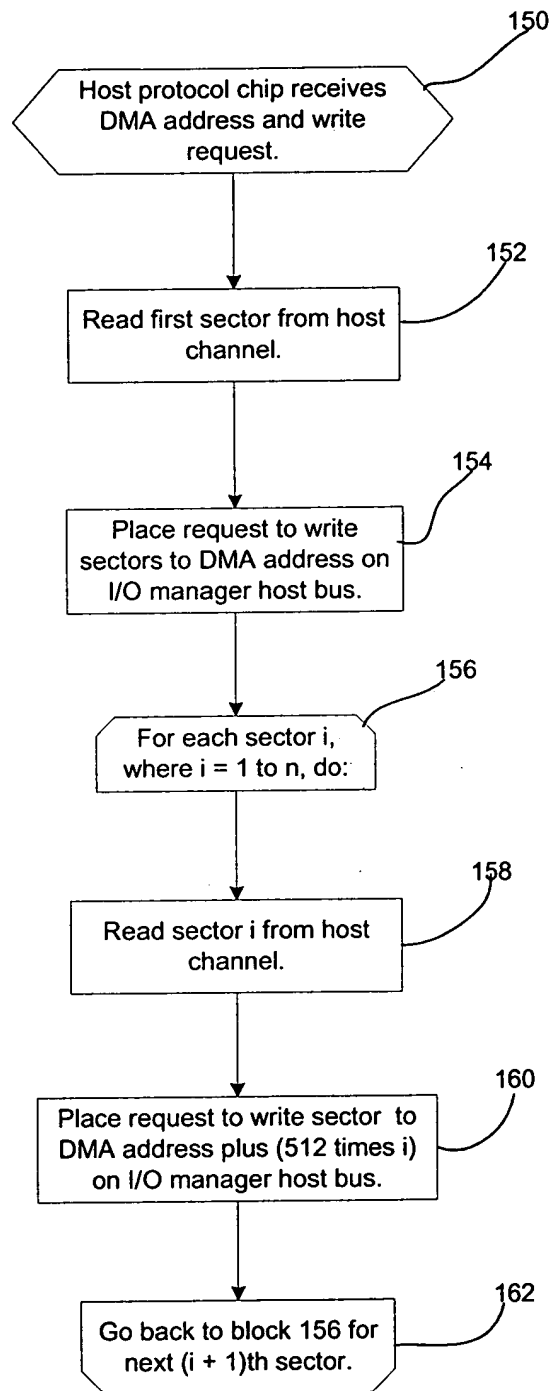


FIG.6

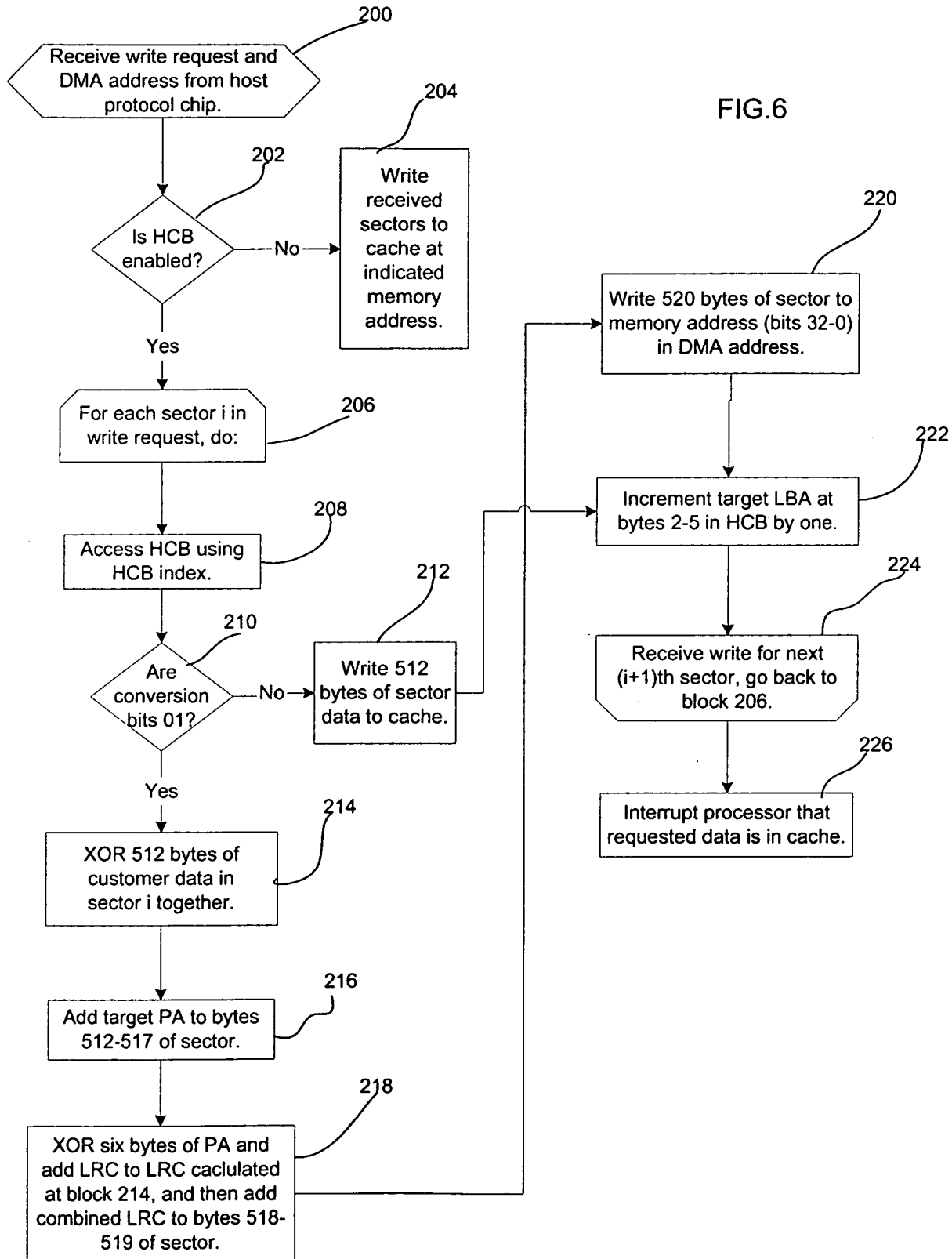


FIG.7

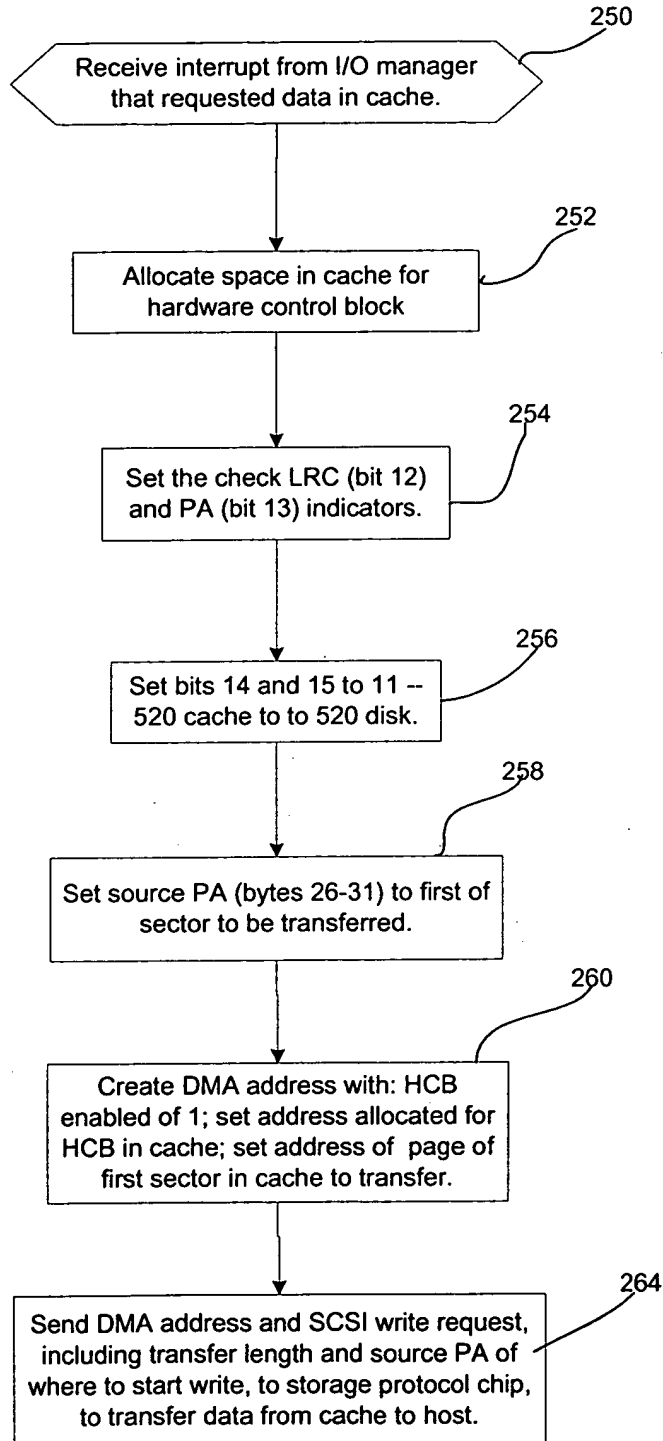


FIG.8

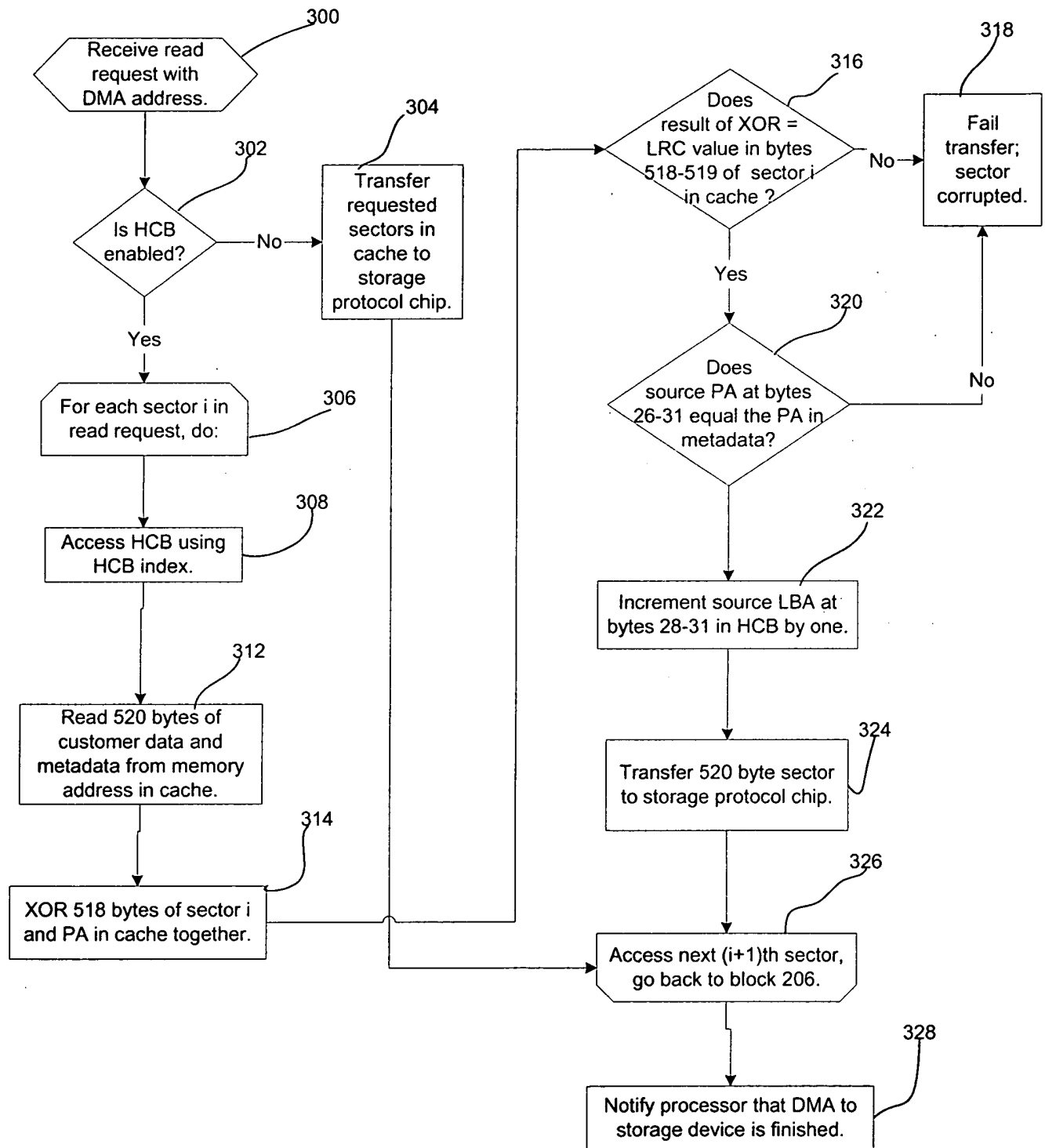


FIG.9

